501.39812VV2

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: YAMAZAKI, et al.

Application No.: TBD

Filed: August 13, 2003

For: FABRICATION METHOD FOR SEMICONDUCTOR INTEGRATED

CIRCUIT DEVICE

Expected

Group: 2822

Expected

Examiner: S. Meier

## INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR § 1.97 AND § 1.98

Mail Stop Patent Application Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450 August 13, 2003

Sir:

Pursuant to Applicants' duty of disclosure, enclosed please find a List, on a form substantially equivalent to Form PTO-1449, of documents cited in connection with prior applications of the above-identified application, that is, Application No. 09/810,577, filed March 19, 2001, and Application No. 09/811,589, filed March 20, 2001.

Since the above-identified prior Application No. 09/810,577 and No. 09/811,589 are being relied upon under 35 USC § 120 in the present application, copies of the listed documents are not enclosed. See 37 CFR § 1.98(d).

This Information Disclosure Statement is being submitted concurrently with the filing of the above-identified application. Accordingly, requirements of

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37 CFR 1.97(b) are clearly satisfied.

Of the documents on the enclosed List, please note that the listed Japanese patent document, and the "OTHER DOCUMENTS" listed, are discussed in the specification of the above-identified application (see page 1 of this specification). Clearly, requirements of 37 CFR 1.98(a)(3) are satisfied, in connection with all documents on the enclosed List

In view of all of the foregoing, it is respectfully submitted that all applicable requirements of 37 CFR § 1.97 and § 1.98 have been satisfied, in connection with all documents on the enclosed List. Accordingly, consideration of the listed documents, upon examination of the above-identified application, is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 501.39812VV2) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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WIS/sjg

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT					YAMAZAKI, et al.			
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	Document Number	Date	Name		Class	Subclass	Filing Date	
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Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date
AA	, , , , , ,	3-2001	Ma, et al.			
Al	, , , , ,	11-2001	Costrini, et al.			
AC	1 1	1-2002	Kitahara, et al.			
AI		2-2002	Berry, et al.			
Al	6,348,420	2-2002	Raaijmakers, et al.			
Al					T	
AC						
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## FOREIGN PATENT DOCUMENTS

Examiner	Document	I.		G,		Translation		
Initial		Number	Date	Country	Class	Subclass	Yes	No
1	AM	11330463	11-1999	Japan				
	AN	2805924	9-2001	France				
4	AO							
	AP							
4	$\overline{AQ}$							
	AR							
	AS							
	AT							

		UMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)				
A		Polysilicon-Germanium Gate Patterning Studies in a High Density Plasma Helicon Souce, 1997 American Vacuum Society, pp. 1874-1880				
A	V	Germanium Etching in High Density Plasmas for 0.18 PM Conplementary Metal-Oxide- Semiconductor Gate Patterning Applications, 1998 American Vacuum Society, pp. 1833- 1840				
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